Attorney Docket No.: MIO 0104 VA/40509.259
Application Number: 10/650,563

Amendments to the Specification:

Please replace the title with the following amended title.

METHOD OF MANUFACTURING A MULTILAYERED DOPED CONDUCTOR FOR A CONTACT IN AN INTEGRATED CIRCUIT DEVICE

Please replace the paragraph [0001] with the following amended paragraph.

This application is a division of U.S. Patent Application Serial No. 10/230,948 filed August 29, 2002, now U.S. Patent 6,670,682, issued December 30, 2003.

Please replace the paragraph [0038] with the following amended paragraph.

Field oxide regions 12 are formed to isolate active areas in which semiconductor devices, such as a transistor, can then be provided in the mesas according to the following processes. In the illustrated embodiment, substrate 10 is a p-type silicon substrate, and the field oxide regions 12 are made of a thermal oxide film having a thickness of from about 2000 to about 5000 Angstroms. The surface of the substrate 10 is thermally oxidized to form the desired ~~field~~ (and/or gate) gate oxide 14 thickness. The thickness of ~~field~~ gate oxide 14 may be from about 30 to about 200 Angstroms.

Please replace the paragraph [0040] with the following amended paragraph.

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Referring to FIG. 3, a layer of photoresist (not shown) is applied over the silicide layer 18 and patterned to form a photoresist mask where gate electrodes and/or interconnecting lines are to be formed. The ~~field~~ gate oxide 14, the polysilicon or polycide layer 16, and the silicide layer 18 are etched away in areas not covered by the mask. An insulating capping layer 20 is then grown or deposited on the top and sidewalls of the remaining layers 14, 16, and 18 to a thickness of between from about 100 to about 200 Angstroms, forming gate structure 22. Capping layer 20 may be a silicon nitride or other insulating material, such that gate structure 22 functions as a word line in a DRAM cell.

Please replace the paragraph [0041] with the following amended paragraph.

The substrate then undergoes a re-oxidation to re-grow field oxide 14R, wherein field gate oxide 14 in the gate structure 22 is the gate oxide. Next, lightly doped source and drain (LDD) regions are formed in the substrate 10 adjacent the channel region. The lightly doped drain (LDD) N- regions are formed by implanting ions 24, selected from phosphorus, arsenic, and antimony ions, at energies within ranges that are conventional in the art to achieve a selected source and drain impurity ion amount.

Please replace the paragraph [0044] with the following amended paragraph.

A material layer is then deposited and partially etched away to leave spacers 32A and 32B on the sidewalls of the gate structure 22, as shown in FIG. 5. The spacers 32A and 32B may have a base width from about 100 to about 500 Angstroms, and comprise silicon oxide, silicon nitride, or any other suitable spacer material.